<u>REMARKS</u>

Objection to the Specification

The abstract of the disclosure is objected to because of the incorporation of figure reference numbers. A new abstract is supplied in this amendment. Therefore, withdrawal of the objection to the specification is respectfully requested.

Claim Objections

Claims 3 and 4 are objected to because of informalities. Specifically, the Examiner is objecting to the phrase "other control unit" and "other control units" in claims 3 and 4. Taking the Examiner's comments into consideration claims 3 and 4 have been amended. Therefore, withdrawal of the objection to claims 3 and 4 is respectfully requested.

Claim Rejections under 35 USC §103

Claims 1-5 are rejected under 35 USC §103(a) as being unpatentable over Grundvig et al. (U.S. Patent No. 6,266,780) in view of Congdon (U.S. Patent No. 6,311,296) and further in view of Cheng (U.S. Patent No. 6,459,705).

The present invention is an abnormality detecting device (600). When a prescribed condition is satisfied, if the abnormality detecting device (600) does not detect the abnormality of a low frequency oscillator (42), a switching device (10a) exchanges the clock pulse for operating a CPU (10) from a first clock pulse (P1) to a second clock pulse (P2) so that the CPU (10) is

shifted to a low power consumed state. When a prescribed condition is satisfied, if the abnormality detecting device (600) detects the abnormality of the low frequency oscillator (42), an exchange stopping device (10b) stops the exchange of the clock pulses by the exchange device (10a).

Grundvig et al. describes in the background of the Related Art Section of the specification that it is well known that a digital circuit requires more power if operated at a higher speed than a lower speed. A faster system clock may be used during times when maximum processing capability is desired. A slower system clock may be used at times of low activity when conservation of power is desired.

Congdon describes in claim 1 a bus monitoring device having a local clock and local reset. The bus monitor is able to monitor the bus for errors or fatal conditions. Congdon also describes the use of a counter.

Cheng describes that a sleeping computer may monitor system voltages and awaken upon a change in status.

The feature of the present invention is that in a system having many control units connected with a bus line, the each control unit includes the first and second oscillators for producing first and second clock pulses for operating the CPU at the first and second frequencies, exchanging means for exchanging clock pulses for operating the CPU from the first clock pulses to the second clock pulses when a prescribed condition is satisfied, thereby shifting the CPU to a low power consumed state, and exchange stopping means for stopping exchange of the clock

pulses if the abnormality detecting means detects the abnormality when said prescribed condition is satisfied. The prescribed condition is that "electric appliances within the vehicle are in a non-operating state when an ignition switch has been turned off and a door has been locked" as described in the specification.

Generally, a system having a CPU is provided with a watchdog timer for monitoring an abnormality of the CPU and outputting a reset signal to return an initial condition the CPU. However, with the low frequency oscillator being out of order, when the CPU shifts to the low power consumed satate, the CPU becomes disabled. After a prescribed period passing, the watchdog resets the CPU. The reset operation of one control unit requests resetting the other control units via the bus line, and all control units shift to a high speed processing state. Thereby, when one of the low frequency oscillator is out of order, whole system cannot shift to the low power consumed state.

According to the present invention, even if one of the low frequency oscillator is out of order, the <u>exchange stopping means</u> stops shifting the CPU to a low power consumed state so that the reset operation by the control unit, in which the low frequency oscillator is out of order, can be stopped.

Cheng teaches that the CPU shifts from the lower power consumed state when it is detected that the oscillator is out of order. All the references relied upon in the rejection do not disclose or teach the feature of the present invention as a prescribed condition, when the detector detects abnormality, exchanging the operation state of the CPU is stopped.

Therefore, amended claims 1 and 5 patentably distinguish over the prior art relied upon by reciting, as exemplified by claim 1,

"A control unit for executing data communication between itself and another control unit, the control unit outputting a signal for resetting said another control unit through a bus line when the control unit is reset, comprising: a CPU which is operated in accordance with a prescribed program; a watchdog timer for monitoring operations of the CPU and outputting a reset signal to return the CPU to an initial condition when an abnormal state of the CPU is detected; a high frequency oscillator for producing first clock pulses for operating the CPU at a first frequency; a low frequency oscillator for producing second clock pulses for operating the CPU at a second frequency which is lower than said first frequency; exchanging means for exchanging clock pulses for operating the CPU from said first clock pulses to said second clock pulses when a prescribed condition is satisfied, thereby shifting the CPU to a low power consumed state; abnormality detecting means for detecting abnormality of the low frequency oscillator; and exchange stopping means for stopping exchange of the clock pulses by said exchanging means if said abnormality detecting means detects the abnormality when said prescribed condition is satisfied." (Emphasis Added)

Therefore, withdrawal of the rejection of Claims 1-5 under 35 USC §103(a) as being unpatentable over Grundvig et al. (U.S. Patent No. 6,266,780) in view of Congdon (U.S. Patent No. 6,311,296) and further in view of Cheng (U.S. Patent No. 6,459,705) is respectfully requested.

U.S. Patent Application Serial No. 09/941,701 Reply to OA dated June 17, 2004

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 1-5, as amended, are believed to be in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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